1K/2K/4K/8K/16K/32K/64K byte
1.8V EEPROM IP Macro Blocks
For 0.18um CMOS Logic Process of Key-Foundry
Product Code: WC18EX2

1. General Description

Key features

- 1.8V Single power supply : 1.62~1.98V
- Fast read cycle time : 12MHz
- x8 read output
- Page size : 64 bytes
- Low active current : 2mA (Typ.) at 10MHz
- Low write current: 1.0mA (typical)
- Page Erase : 4msec (typical)
- Byte or page program : 4msec (typical)
- Extra user memory (XUM) : one page size for special user purpose
- Main functions : read, page-erase, and page-program
- Test modes : even/odd /all page-erase, even/odd/all page-program, and verify mode
- Device reset by RSTn pin (during power-up and power-down)
- Data retention : More than 10 years

“W18EX2” is a 2P3M (two-poly, three-metal), non-volatile EEPROM Macro IP block which is embedded into the 0.18um standard CMOS logic process of Key-Foundry.
Two versions of W18EX2 Macro blocks are available: **WC18EX2** is for “Generic process (G)” and “Low-power process (W)”. Both versions have exactly the same functionality, except operational temperature and standby current. Refer to the difference table in table 1.
Each EEPROM IP block has **64 bytes** per page for writing data to the main memory. Furthermore, an additional memory area (called “**Extra User Memory**”) with a page is provided, which can be used for storing specific codes or user information.

Table 1. Difference between WC18EX2G and WC18EX2W

	Macro IP code	WC18EX2	
	Process type	Generic (G)	Low power (W)
	Process name of Key-Foundry	HM18E	HM18EW
Operational Temperature	Read	-40C ~ 85C	-40C ~ 85C
	Write	-20C ~ 85C	-20C ~ 85C
Stand-by Current (Vcc=1.98V)	Typical (25C)	30uA	30uA
	Max. (85C)	100uA	60uA
Deep power-down current (Vcc=1.98V)	Typical (25C)	< 1uA	< 1uA
	Max. (85C)	70uA	30uA

Table 2. Product code and access time

Product Code		Density	Read cycle time (tRC)	Page size for write	Output width for read
G-version	WC18EX2G_1K	1Kbytes	16MHz	64bytes	x8
	WC18EX2G_2K	2Kbytes			
	WC18EX2G_4K	4Kbytes			
	WC18EX2G_8K	8Kbytes			
	WC18EX2G_16K	16Kbytes			
	WC18EX2G_32K	32Kbytes	12MHz		
	WC18EX2G_64K	64Kbytes			
W-version	WC18EX2W_1K	1Kbytes	16MHz	64bytes	x8
	WC18EX2W_2K	2Kbytes			
	WC18EX2W_4K	4Kbytes			
	WC18EX2W_8K	8Kbytes			
	WC18EX2W_16K	16Kbytes			
	WC18EX2W_32K	32Kbytes	12MHz		
	WC18EX2W_64K	64Kbytes			

Fig 1. Circuit block diagram

Circuit Block Diagram

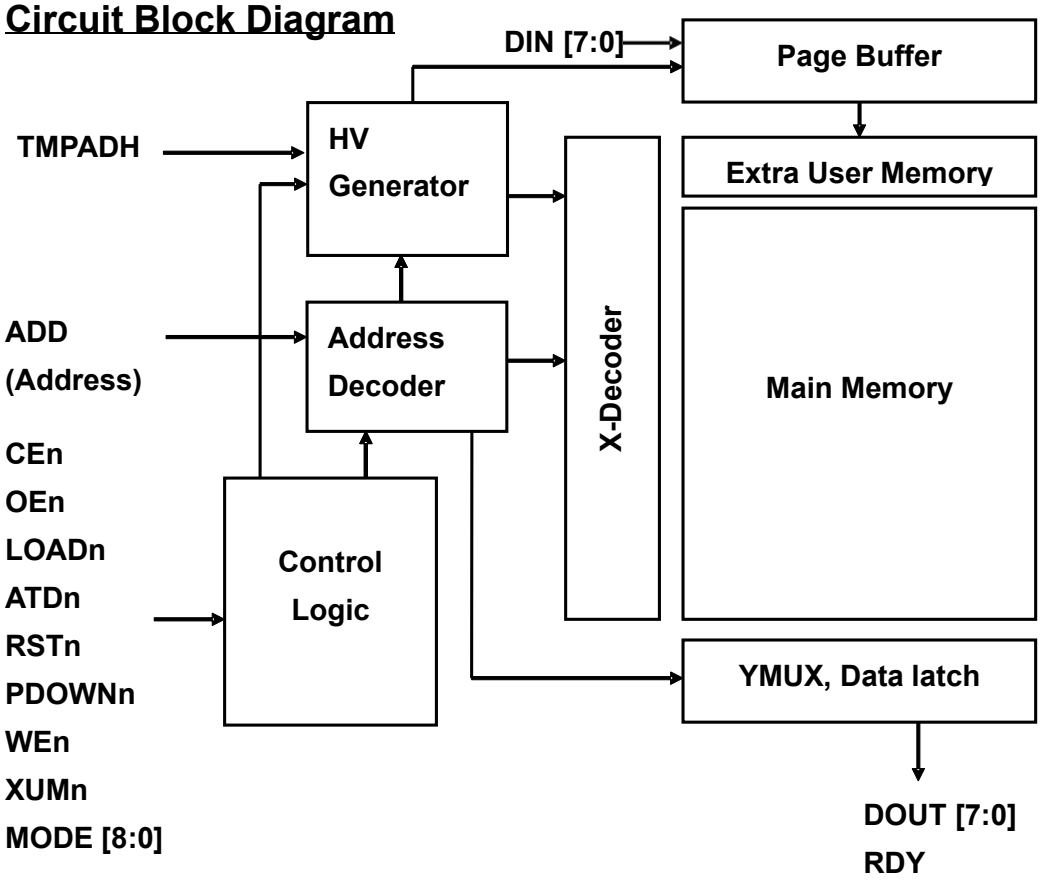


Table 3. Signal description

Symbol	Pin name	Function
MODE[8:0]	Mode select bits	To select the functional modes
XUMn	Extra User Memory Enable	To select the extra user memory (when XUMn = Low)
ADD[A_{MS}:0]	Address inputs	Memory addresses.
DIN [7:0]	Data inputs	To receive input data for write.
DOUT [7:0]	Data outputs	Output data from EEPROM IP.
CEn	Chip Enable	To activate the EEPROM macro device.
OEn	Output Enable	“Don’t Care” Pin
WEn	Write Enable	To control write operations.
RSTn	Reset Enable	To reset the device during power-up or terminate any operation under progress. All internal registers including the page buffer are reset by RSTn.
LOADn	Load Enable	To load data into page buffer for a write operation
RDY	Ready	To determine when a write operation is completed. RDY=high for “ready to read”, and low for “busy during write operation”.
PDOWNn	Power-down mode Enable	“ PDOWNn = low” forces the IP block to enter “power-down mode”. In this mode, the current consumption is deeply suppressed down to 1uA, typically.
ATDn	Address transition Detector Enable	This signal is used for for “ATD (Address Transition Detect) pulse”.
TMPADH	Test Pin	High Voltage Measure

Note 1) A_{MS} : The Most Significant Address Bit
Note 2) Here, “write” means erase or program, or both operations.

2. Functional Modes

Two groups of functional modes are provided: **Main modes** and **Test Modes**. These functions can be selected by MODE [4:0] as shown in the table 4. Main functions are composed of five functions: Reset, Stand-by (and Power down Mode), Read, Page-erase and Page-program. These main functions are enough to meet almost all functional requirements of the normal customers for their various applications. On the other hand, test modes can be usefully utilized in many cases like customer’s production test.
To correctly write data into the main memory space, data should be first loaded with a specific address into an internal register called a **page-buffer**. This “data load operation” is performed during **“Load cycle**”. And then **“**actual erase” should be executed on a selected page. Finally**,** the data loaded in the page-buffer should be programmed into the main memory space.
In this datasheet, “write operation” means “erase” or “program”, or both for convenient description. However, as shown in the table 4, “load cycle” is one part of write operation. This is because “write operation” starts automatically once after the load cycle is completed. So, “load cycle” can not be performed or executed separately from the write operation.
In other word, in the table 4, all “page-erase” or “page-program” is actually composed of two internal cycles respectively.

- page-erase → Load + Erase
- page-program → Load + Program

Table 4. Functional modes and Mode selection bits (MODE[4:0])

Mode	Functions		MODE [4:0]
Main Mode	Reset		don't care
	Standby (and Power Down Mode)		
	Read		00h
	Page-erase (load + erase)		04h
	Page-program (load + program)		08h
Test Mode	Write	All Page Write	0Fh
	Erase	Even page-erase	05h
		Odd page-erase	06h
		All page-erase (Bulk erase)	07h
	Program	Even page-program	09h
		Odd page-program	0Ah
		All page-program (Bulk program)	0Bh
	Verify	Erase-verify	14h
		Program-verify	18h

Table 5. Pin description and status for main modes

	Main Modes						
	Power Down	Reset	Standby	Read	Write operations		
					Load	Page Erase	Page Program
MODE[4:0]	x	x	x	00h	04h (erase), 08h (program)	04h	08h
XUMn	x	x	x	H	H	H	H
ADD [byte]	x	x	x	Ain	Ain	x	x
ADD [page]	x	x	x	Ain	Ain	Ain	Ain
Din[7:0]	x	x	x	x	Din	x	x
DOUT[7:0]	x	x	x	Dout	x	x	x
CEn	H	H	H	L	L	L	L
OEn	x	x	x	x	x	x	x
WEn	x	x	x	H	L	H	H
LOADn	x	x	x	H	L	H	H
RSTn	x	L	H	H	H	H	H
PDOWNn	L	H	H	H	H	H	H
ATDn	x	x	x	Toggle	H	H	H
RDY	H	H	H	H	H	L	L

(Note 1) x (Don't care): Vil or Vih for Input, Vol or Voh Out for output.
(Note 2) Ain : Address Input
(Note 3) ATD (Address Transition Detect) signal is internally generated by ATDn pulse (Toggle) in read operation

3. Read

The EEPROM Macro device automatically enters the read mode after power-up. During power-up, RSTn (Device Reset Signal) should be kept low to correctly initialize the device.

The device has two control pins (CEn and ATDn) for read, which must be correctly asserted in order to obtain valid data at the outputs. Chip Enable (CEn) is used for enable the device. ATDn is used to generate an internal ATD (Address Transition Detect) for the input addresses.
Output Enable (OEn) is "don't care" to the output pins. In case that addresses are kept stable, ATDn to Valid output time (tATO) is defined as a delay from the rising edge of ATDn to the valid data output. Resultantly, actual read access time is the sum of tATD and tATO".

Fig 2. Read Operation Timing Diagram

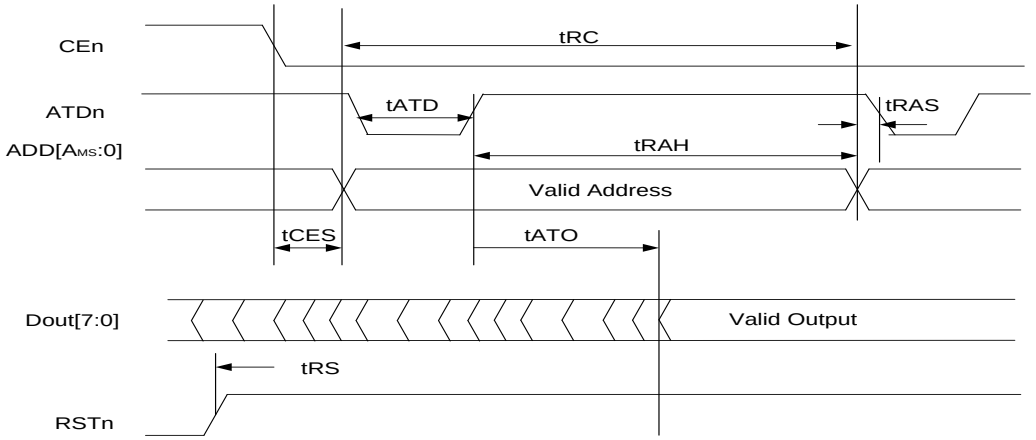


Fig 2-1. Burst Read Timing Diagram

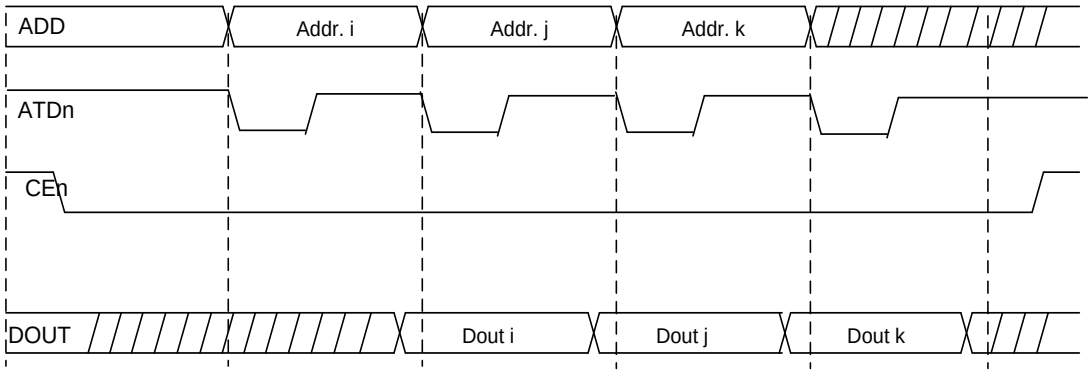


Table 6.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRC	Read Cycle Time			12	MHz
tATD	ATDn Low Width Time	40			ns
tRAS	Read Address Setup Time	0			ns
tRAH	Read Address Hold Time	40			ns
tATO	ATDn High to Valid Output Time			40	ns
tCES	CEn Setup Time	400			ns
tRS	RSTn Setup Time	100			ns

Note 1) tRC, tATD, tRAS, tRAH and tATO depend on the size of the device (Table 2).
Note 2) For read access time, **Cload** (Load Capacitance at output) is assumed to be less than **0.3pF**.

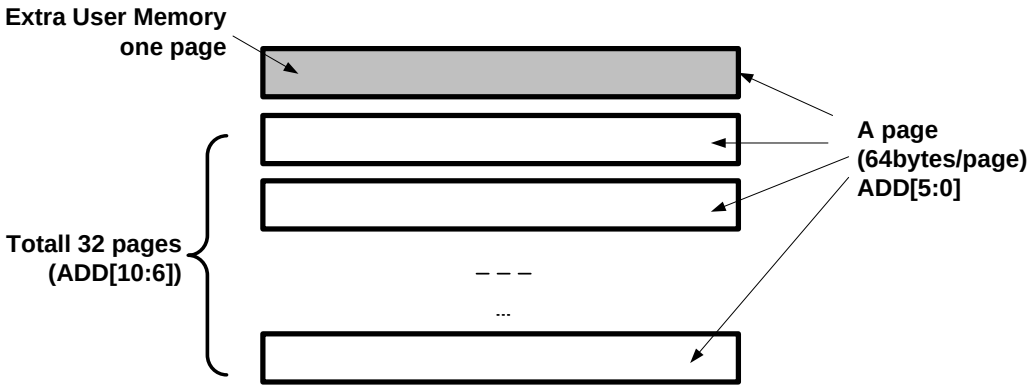
4. Physical organization of Main memory

A page is composed of 64 bytes. The whole memory array is composed of a lot of pages. And, an extra memory space (one page size) is additionally available for users' special usage. This special memory is called "Extra User Memory (XUM)". Refer to table 7 and Fig. 3 to see how physically bytes and pages are organized into the whole memory array.

Table 7. Byte address, page address, and number of pages

Product code	Memory size (Bytes)	Page size	Byte address	Page address	Number of pages
WC18EX2_1K	1K	64 bytes	ADD[5:0]	ADD[09:6]	16
WC18EX2_2K	2K			ADD[10:6]	32
WC18EX2_4K	4K			ADD[11:6]	64
WC18EX2_8K	8K			ADD[12:6]	128
WC18EX2_16K	16K			ADD[13:6]	256
WC18EX2_32K	32K			ADD[14:6]	512
WC18EX2_64K	64K			ADD[15:6]	1K

Fig. 3 Physical organization of bytes and pages (2Kbytes Macro block for an example)

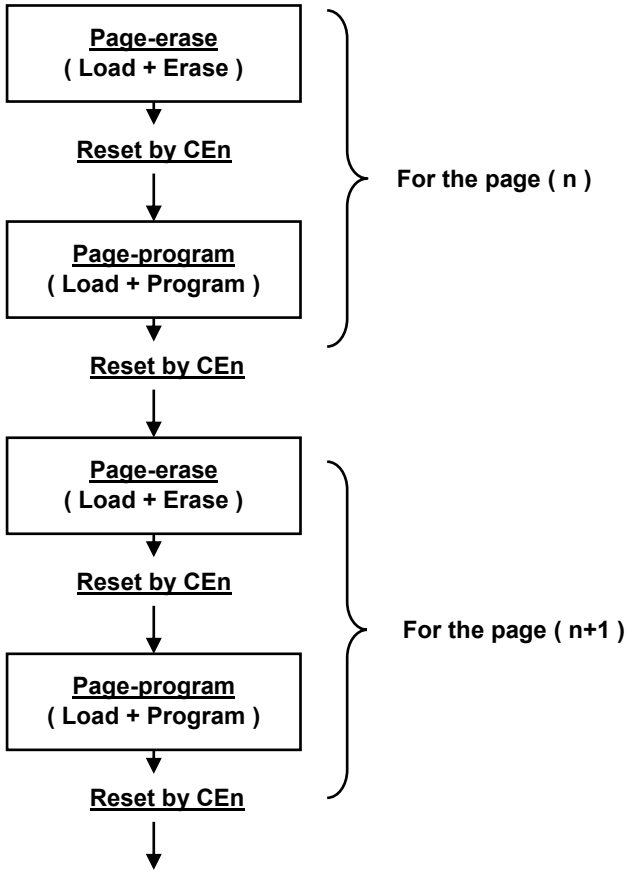


5. Write Operation

In this device, two types of write operation are provided: page-erase and page-program. Each write operation is composed of two internal cycles: Load and write. In order to correctly update data, the page selected by user should be first erased, and then “user data” should be properly programmed into the selected page in the main memory array. Here, it should be noted that “**device reset by CEn**” is required before moving to next write operation. This device reset is necessary for clearing the page-buffer which affects actual write operation. Refer to Fig.4.

The page-program or page-erase in the main mode is basically performed on a specific single page which was selected by a page address during load cycle. However, write functions in the test mode differently work, where even, odd or all pages are parallel written at once (Refer to table 9 and table 10).

Fig. 4 Normal Write Operation Sequence based on “page-by-page”



RDY, a Staus bit for Write Operation

The “data load cycle” is controlled by “LOADn”, and “the load cycle” is automatically followed by the next write operation like erase or program.
“RDY signal” is a status bit for write operation (erase or program).This signal can be usefully utilized to check or monitor when the write operation actually starts or when it is completed. **“**Data load” is terminated by driving “LOADn” from low to high. Then, “actual write operation” starts, tBUSY later after LOADn goes high. At the same time, “RDY” goes low to indicate that “write operation is under progress. The write operation (erase or program) is executed for typically 4msec (tWRITE). Since the same physical mechanisms are used in program and erase operation, “write time” is also the same for both. As soon as the write operation is competed, RDY returns to High. During the whole write operation, the page and byte address should be kept stable, as shown in the Fig.5. Here, 4msec (typical value) of write time (tWRITE) is internally set, so the write time (tWRITE) cannot be changed or controlled by users in this main page-erase mode. Refer to Fig. 5.

Device Reset by “CEn”

Actual write operation is directly affected by the data loaded into the page-buffer.
So, “page-buffer reset” is necessary before moving to the next write. As shown in the Fig. 5, the entire write operation (load + write) is performed while “CEn” is kept low. However, when CEn is driven from low to high once after the write operation is done, the device is immediately reset including the page-buffer and then returns to the normal read. Furthermore, when CEn is driven to high while a write operation is in progress, the write operation is immediately terminated and returns to read mode. At the same time, the page-buffer is cleared by CEn reset.

Fig. 5

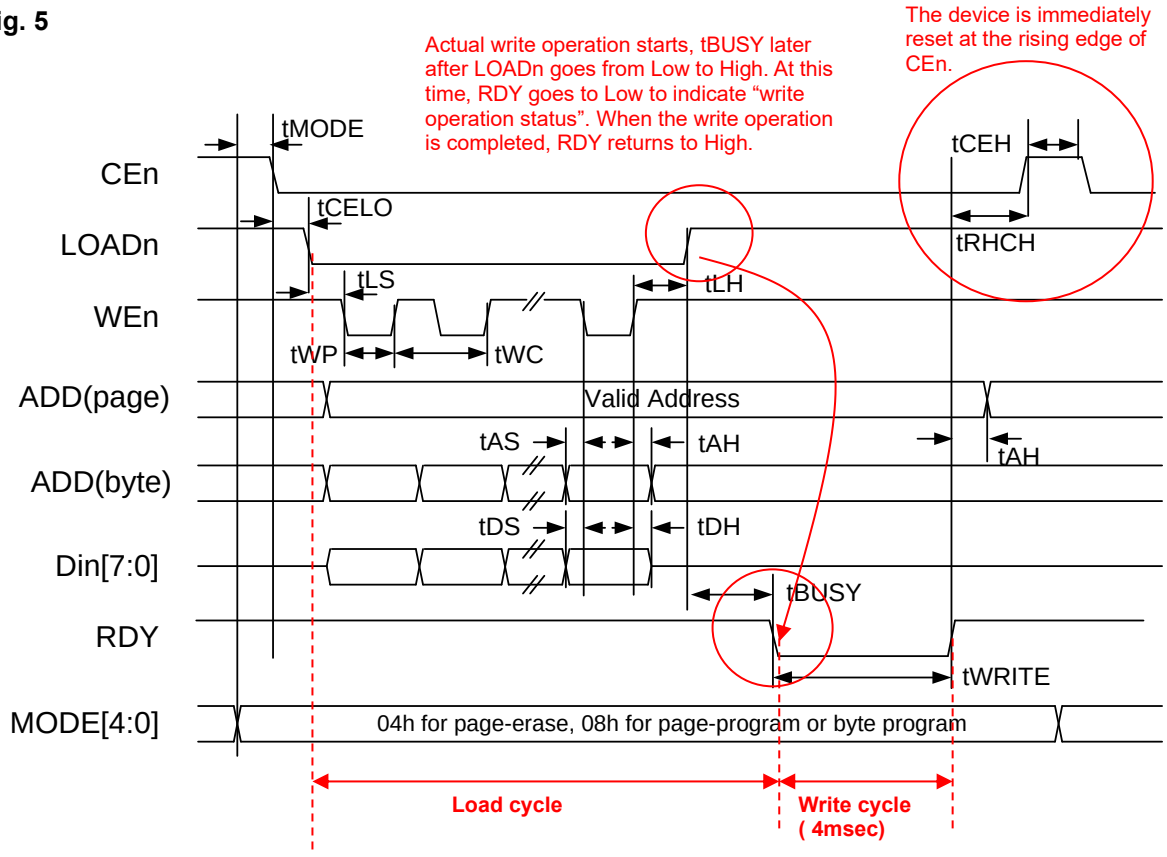


Table. 8

Symbol	Parameter		Min.	Typ.	Max.	Unit
tWC	Write Cycle Time		50			ns
tWP	Write Pulse Width		20			ns
tAS	Address Setup Time		5			ns
tAH	Address Hold Time		5			ns
tDS	Data Input Setup time		5			ns
tDH	Data Input Hold time		5			ns
tMODE	MODE pin Setup Time		0			ns
tCELO	CEn Low to LOADn Low time		0			ns
tRHCH	RDY High to CEn High time		0			ns
tCEH	CEn High Width		20			ns
tLS	LOADn Setup Time		50			ns
tLH	LOADn Hold Time		50			ns
tBUSY	RDY "low" Delay Time		200			ns
tWRITE	Write Time	Page-erase	3	4	8	ms
		Page-program	3	4	8	ms

6. Page-erase

In this EEPROM Macro block, erase is performed on a specific page which is addressed by user during the load cycle. However, it should be noted that "byte erase" is not supported. Only "page erase" is supported. In order to correctly write data into the main memory array, a memory area of the selected page should be first clearly erased before any data is programmed there later.
Actually, a page-erase operation is composed of two separate internal operations: Load and Erase. As shown in the Fig.4, during the load cycle, "data" should be first written into the page-buffer while LOADn stays at low. At the same time, the **address of the page location** user wants to erase should be given and kept stable until the whole write operation is completely finished.

More than one byte of data into the page-buffer

Initially, the page buffer is reset to all "0 (erased status)" after power-up. Or it can be reset by "CEn' or can be intentionally reset by RSTn. Data should be first loaded into the page-buffer before any actual write operations start. Any number of bytes can be loaded in **any order** from one byte to the maximum number of bytes (a page-buffer size). In a page-erase operation, "content of byte-data" does not have actual meaning, but **more than one byte of data** at least should be loaded into the page-buffer to activate the next erase operation. If none of byte is loaded into the page-buffer during the load cycle, nothing is erased.

7. Page-program

In the device, a program operation (called “page-program here) is performed on “page-by-page”. One page is composed of 64 bytes regardless of the device density. At first, “byte-data with byte-address” and “page-address” should be loaded into an internal page-buffer during the load cycle. During this load cycle, CEn and LOADn should be kept low while OEn is “Don’t Care”. Any number of bytes can be loaded into the page buffer in any order. Furthermore, any byte-data can be “over-written” into the same byte location in the page-buffer. But, some special care is needed for such a “data over-write”. Byte-data is loaded into the internal page-buffer at the rising edge of WEn while LOADn is kept low. “Data load cycle” is terminated by driving LOADn to high.

As soon as the load cycle is done, actual program operation automatically starts, tBUSY later once after LOADn is driven to high from low. The multiple bytes loaded in the page-buffer are parallel programmed at once into the main memory array. However, the write time is internally fixed at 4msec (typically) regardless of the number of bytes. In other word, the write time cannot be accessed or changed by user. If only one-byte is loaded, what we call “**byte-program**” can be realized. Refer to Fig.5 and Fig.7.

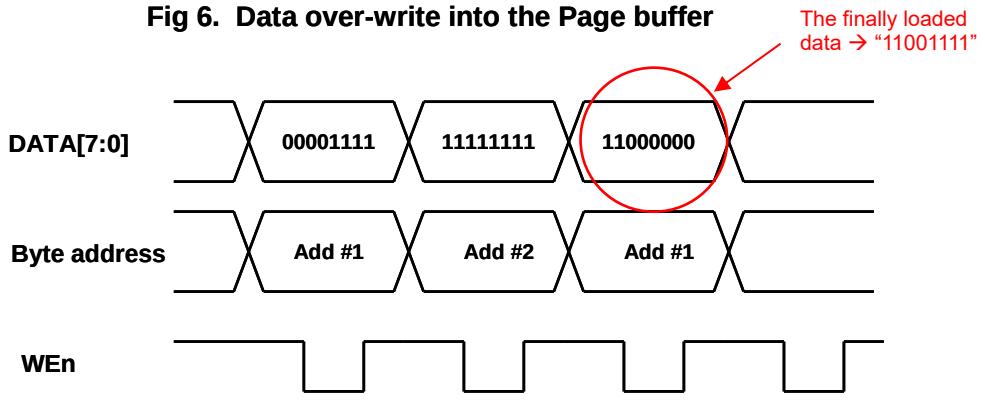
Data and Address

There are two types of address: byte address and page address.
During data load operation, byte-data and byte-address are latched at the rising edge of WEn. However, data and address should be carefully kept stable for the low period of WEn. Refer the timing parameters in Fig.5: tAS, tAH, tDS, and tDH.
Especially, “the page address” should not be changed for the entire period of write including “load cycle”. This stability of the page address is required to guarantee correct data to be written into the actual memory array. If not, data will be written into an unwanted location of page.

Data ‘Over-write” in the page-buffer

In some cases, different data may be tried to be loaded into the same byte location with the same address in the page-buffer. Such a case is called “data over-write”. In such an over-write, only the last loaded data gets valid. However, even if “data over-write” occurs, **“1 bit ” cannot be changed back to “0 bit”**. Only “0 bit” is allowed be changed to “1 bit” in any case. Therefore, special care is required for “data over-write” while loading data into the page-buffer. Refer to the Fig 6 for an example. In this the example, “data over-write” is tried in the byte-address #1. The first try was “data 00001111” and the second try was “data 11000000”. However, the data finally loaded into the page buffer will be “**11001111**” because the previous “1” bit cannot return back to “0”. Therefore, “data over-write” should be carefully preformed. In case that some different data needs to be newly loaded at the same address in the page buffer, just do it after resetting the page buffer by RSTn or CEn

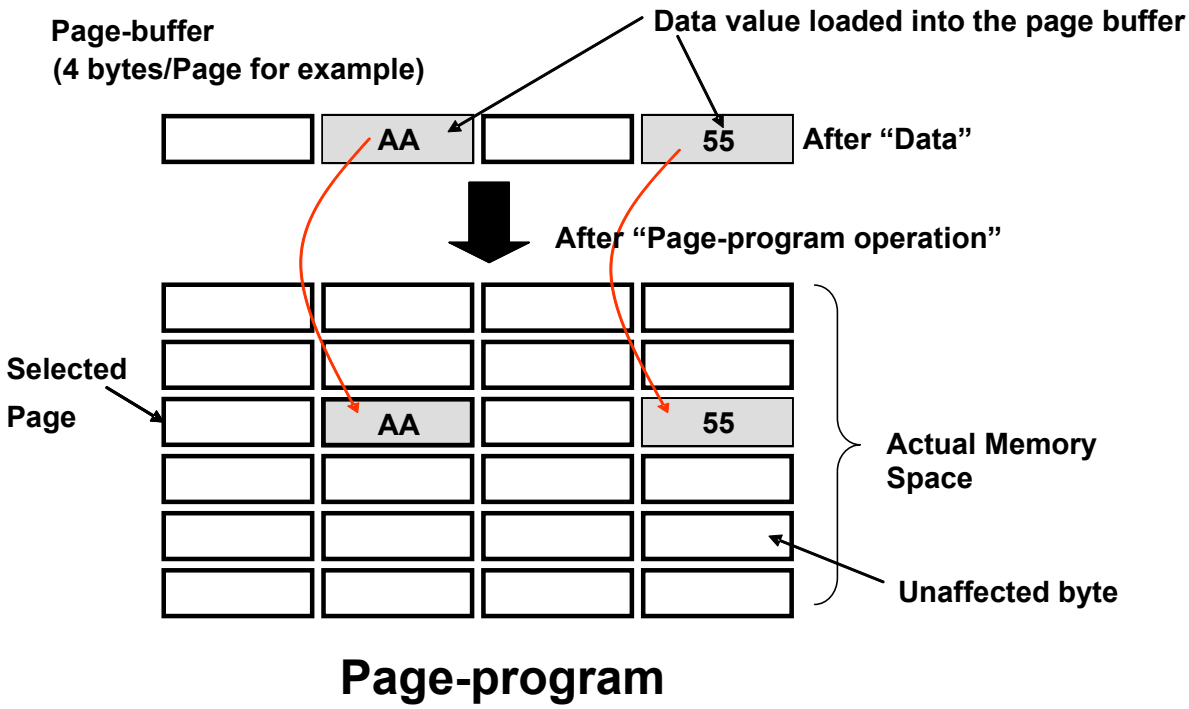
Fig 6. Data over-write into the Page buffer



Data 'Over-write" in the actual main memory

Sometimes, new data can be over-written onto the previous data in the main memory array during the page-programming operation. This is the so-called "over-write" or "over-programming" in the actual main memory. Just like the over-write in the page-buffer (previously described), only "0 bit" can be changed to "1bit" while "1 bit" is not allowed to return to "0 bit" by the page-program operation. Instead, "1 bit' can return to "0 bit" only by performing "erase operation".
Therefore, the page should be previously "erased" by "an erase operation" before any page-program is performed, in order to keep integrity of data.

Fig. 7 Page-program



Page-program

8. Test Modes (Erase)

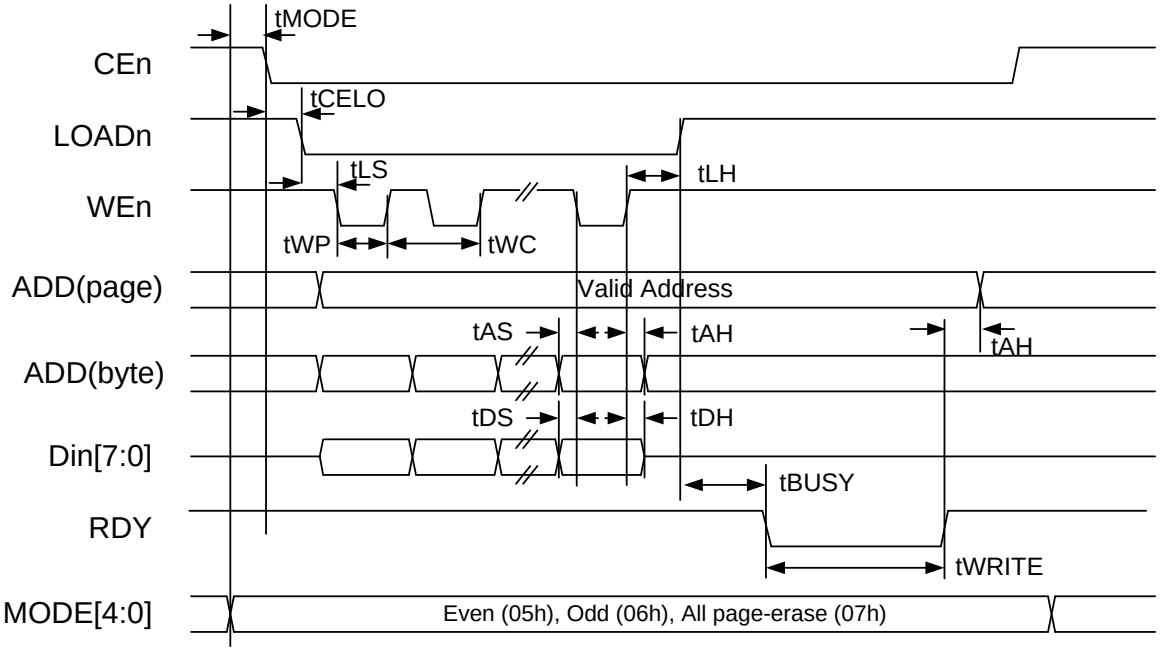
Three test erase-modes (even, odd and all page-erase) are additionally provided for more flexible user application and test-time reduction, and they can be selected by MODE [4:0] as shown in the table 9 below. Each test erase mode is functionally the same as the page-erase operation of the main mode, except that the scopes of pages supported by test modes are different from the main mode, as shown in the table 9 below.

In order to let “actual erase operation” started, more than one byte of data at least should be loaded into the page-buffer during load cycle. If nothing is loaded, none of page is erased.
Refer to Fig.8 for the timing diagram of test erase mode.

Table 9.

Type	Modes	MODE [4:0]	Scope of pages to erase
Main mode	Page-erase	04h	Any single page designated by a page-address
Test mode	Even page-erase	05h	All pages only with even page-address (Page #0, #2, #4…)
	Odd page-erase	06h	All pages only with odd page-address (Page #1, #3, #5...)
	All page-erase (**Bulk erase**)	07h	All pages (Whole memory block)

Fig. 8 Timing diagram for the test erase-modes



9. Test Modes (Program)

Three test program-modes (even, odd and all page-program) are additionally provided for more flexible user application and test-time reduction, and they can be selected by MODE [4:0] as shown in the table 9 below. Each test program mode is functionally the same as the page-program operation of the main mode, except that the scopes of pages supported by the test modes are different from the main mode, as shown in the table 10 below.
In the even or odd-page program mode, the byte-data pattern loaded in the page-buffer is exactly copied (written) into all pages respectively with even, odd or all page-address in the whole memory array block.
On the other hand, the whole memory block can be programmed at once with the same data pattern by performing “all page-program (bulk program)”. However, it should be noted that only “0 bit” can be programmed into “1 bit (programmed state)” by the program operation. So, an ease operation needs before any program operation is performed. The erase operation clears any bit to “0 bit (erased state)”.

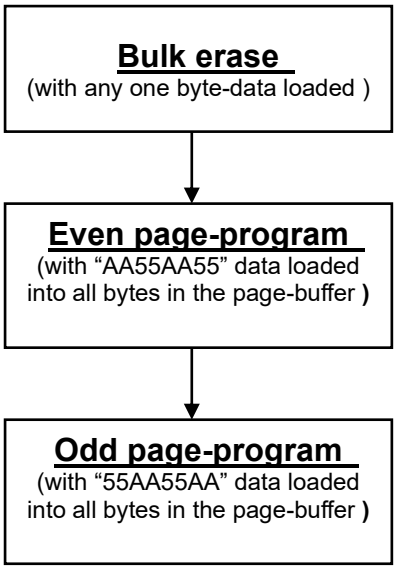
Table 10.

Type	Modes	MODE [4:0]	Scope of pages to program
Main mode	Page-program	08h	Any single page designated by a page-address
Test mode	Even page-program	09h	All pages only with even page-address (Page #0, #2, #4…)
	Odd page-program	0Ah	All pages only with odd page-address (Page #1, #3, #5...)
	All page-program (**Bulk program**)	0Bh	All pages (Whole memory block)

How to generate “CKB (Checker Board) pattern” by using the test modes

A CKB pattern can be easily and fast generated by properly using the test mode functions.
Refer to the block diagram (Fig. 9) below.
First, “bulk erase (all page-erase)” is performed. In this bulk erase, one byte of data at least should be loaded into the page-buffer during the load cycle. And then, an even page-program is executed with data “AA55AA55”. Finally, an odd page-program is executed with data “55AA55AA”. Then, “full CKB pattern” will be easily obtained over the whole memory block. The total write time for the full CKB pattern is about 12msec (typically), regardless of the EEPROM macro device density: bulk erase (4msec), even page-program (4msec), and odd page-program (4msec).

Fig. 9 Fast generation flow for full CKB pattern



10. Verify Mode

In the test mode, two special read modes are provided: **erase-verify** and **program-verify**. Their operations are very similar with read, but their internal operations are clearly different from the normal read. In the device, some reference levels are internally set, respectively for erase and program. These verify functions are operated on each reference level. They can be used in testing or sorting the EEPROM macro device, or for some other special purpose.

The verify modes are activated by setting MODE [4:0] to **14h** (erase-verify) or **18h** (program-verify), in the table 4. The verify operation is controlled by ATDn. Data (verified data) is sensed out while ATDn pulse stays at low (tVTD), and then the data is latched at the rising edge of ATDn. The latched data gets available at output, tATO later from the rising edge of ATDn.
During this verify operation, CEn should be constantly kept low to make the device and its output enabled. However, at least, **50usec of set-up time (tVFD)** is required for the device to get ready for starting the verify operation. The set-up time (tVFD) is defined as the time between the falling edge of CEn and the first falling edge of ATDn.

Fig. 10 Verify timing diagram

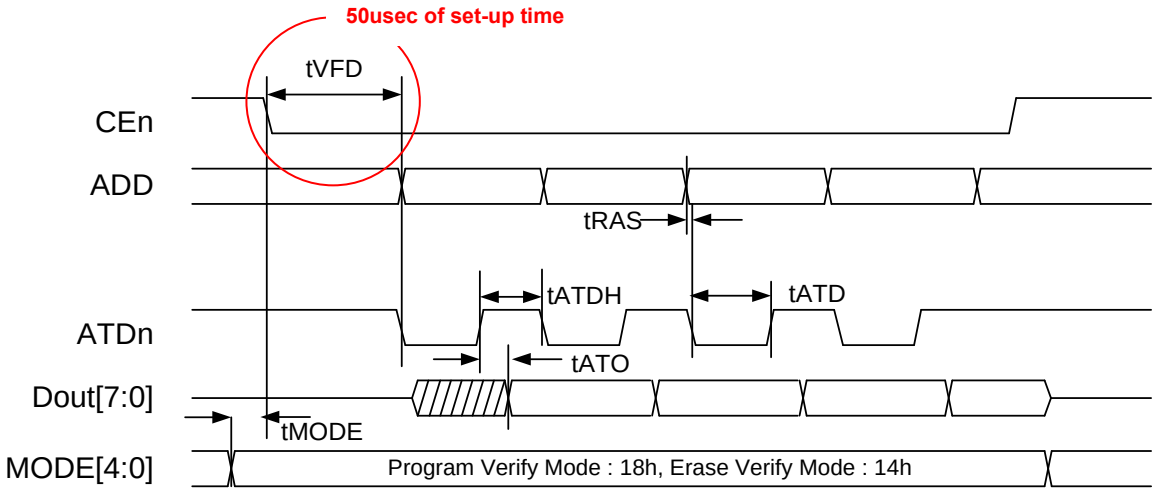


Table 11.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tVFD	Verify Set-up Time	50			us
tATD	ATDn Pulse Low Width	40			ns
tVAS	Address Set-up Time	0			ns
tVAH	Address Hold Time	40			ns
tATO	ATDn High to Valid Output Time			40	ns
tMODE	MODE pin Setup Time	0			ns
tATDH	ATDn Pulse High Width	40			ns

11. User-Time Controlled Write (ATDn)

The period of the write time (the page-erase or page-program) is internally fixed to 4msec, which is not allowed to be changed by users. But, in the user-time controlled write mode driven by ATDn signal, erase or program time can separately controlled by users, just by increasing or decreasing the low duration of ATDn as shown in Fig 11. This special write mode may be very useful especially when it is used for some special user purposes, like product test, verification, and enhancing the reliability in some cases.

After the user-time controlled write is terminated by driving ATDn to high from low, at least **20us of recovery time** (**tREADY**) is required to get out of the internal high-voltage write operations to return to the normal read mode.

Fig 11. Timing diagram of user-time controlled write by ATDn

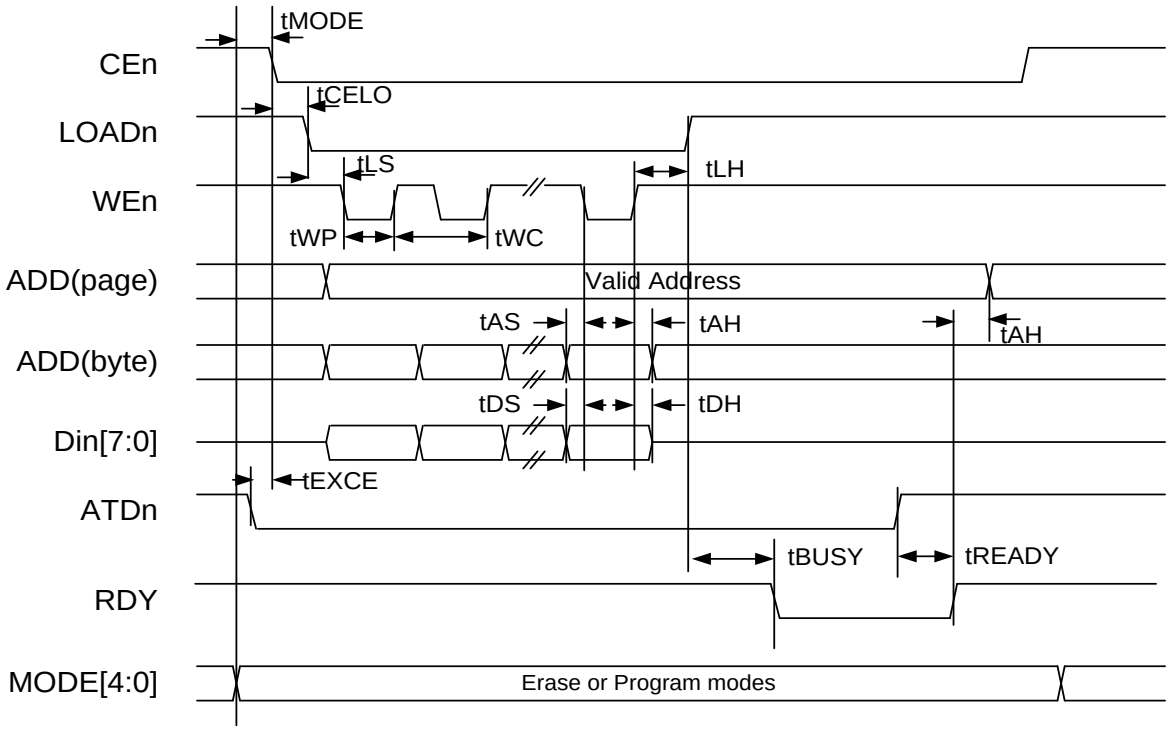


Table 12.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tWC	Write Cycle Time	50			ns
tWP	Write Pulse Width	20			ns
tAS	Address Setup Time	5			ns
tAH	Address Hold Time	5			ns
tDS	Data Input Setup time	5			ns
tDH	Data Input Hold time	5			ns
tMODE	MODE pin Setup Time	0			ns
tCELO	CEn Low to LOADn Low time	0			ns
tLS	LOADn Setup Time	50			ns
tLH	LOADn Hold Time	50			ns
tBUSY	RDY “low” Delay Time	200			ns
tREADY	RDY “high” Delay Time			20	us
tEXCE	ATDn Setup Time		0		ns

12. Extra User Memory (XUM)

One page size of extra memory is provided for users’ specific purposes like storing test codes, product code, or some security serial numbers. As long as XUMn is at High, the extra user memory is not selected. But, in case that XUMn is Low, only extra user memory is selected for the main modes. But, both memories (Main and Extra) are selected at the same time for the test modes. For example, when a bulk erase is performed with XUMn=Low, the extra user memory as well as the main memory is erased at once. Refer to the table 13, Fig 12 and Fig 13.

Table 13.

<table>
<tr><th colspan="2">Mode</th><th>Functions</th><th>XUM=High</th><th>XUM=Low</th></tr>
<tr><td colspan="2" rowspan="3">Main Mode</td><td>Read</td><td rowspan="9">Applied only to “main memory”</td><td rowspan="3">Applied only to “extra user memory”</td></tr>
<tr><td>Page erase</td></tr>
<tr><td>Single byte or page-program</td></tr>
<tr><td rowspan="6">Test Mode</td><td rowspan="3">Erase</td><td>Even page-erase</td><td>Applied only to “extra user memory”</td></tr>
<tr><td>Odd page-erase</td><td rowspan="2">Applied to both memory areas: “main memory” and “extra user memory”.</td></tr>
<tr><td>All page-erase</td></tr>
<tr><td rowspan="3">Program</td><td>Even page-program</td><td>Applied only to “extra user memory”</td></tr>
<tr><td>Odd page-program</td><td rowspan="2">Applied to both memory areas: “main memory” and “extra user memory”.</td></tr>
<tr><td>All page-program</td></tr>
</table>

Fig. 12 Extra user memory

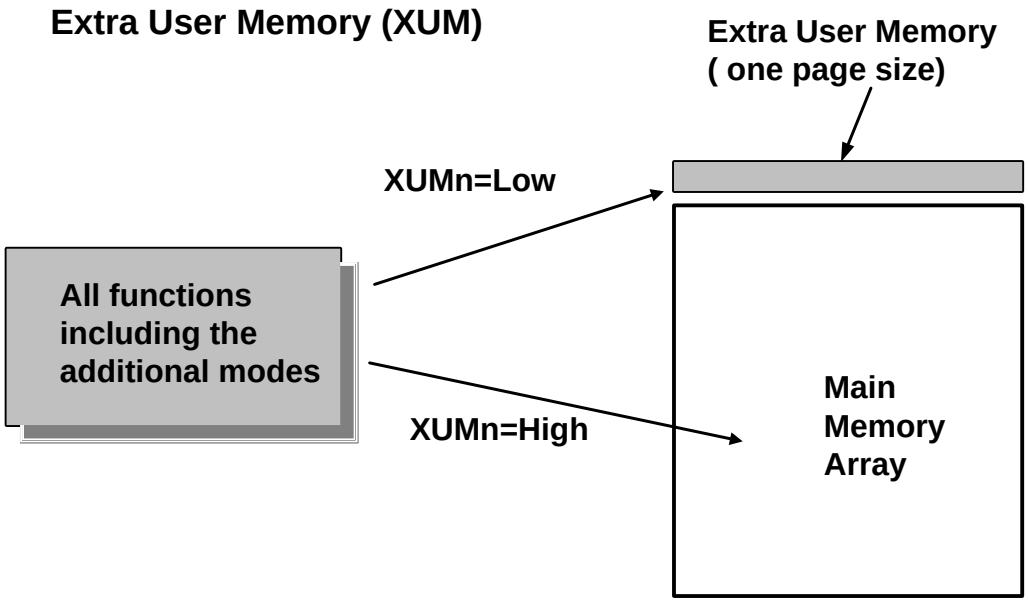


Fig. 13 Extra User Memory

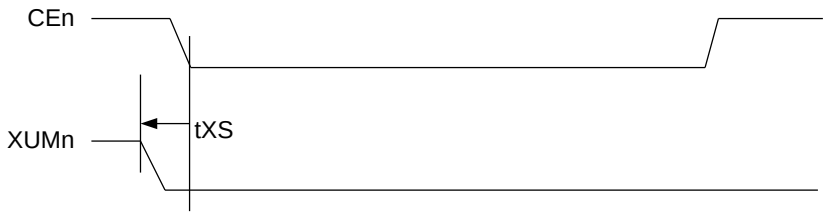


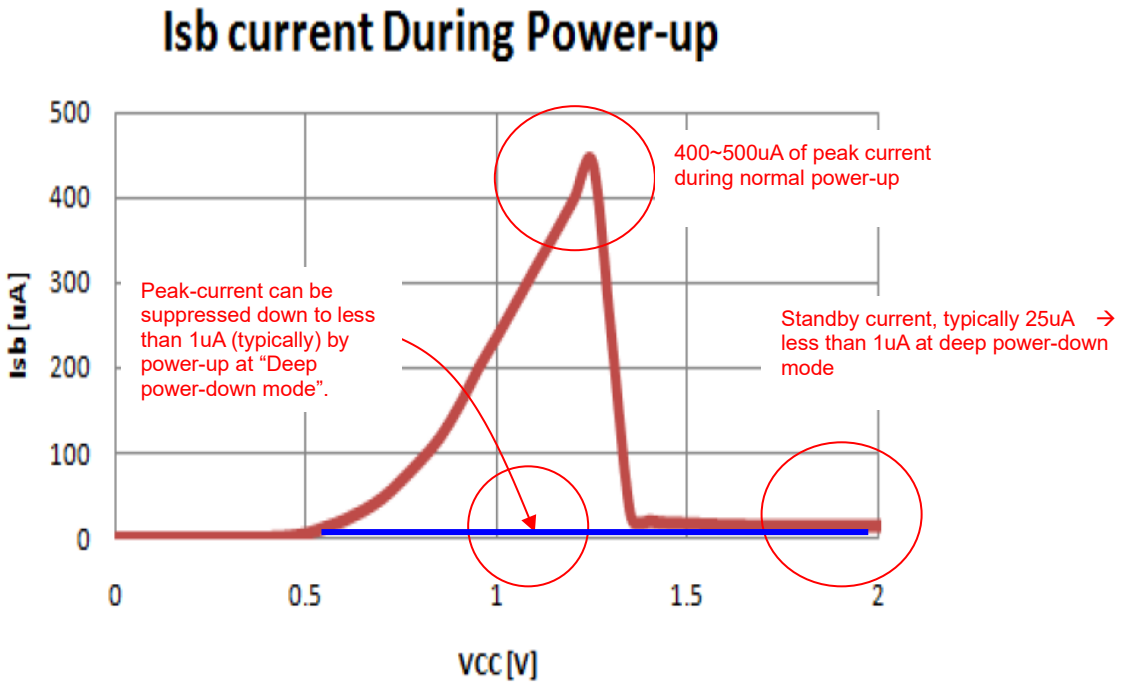
Table 14.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tXS	XUMn Setup Time	30			ns

13. Stand-by and Power Up

The IP block is placed into the standby mode by applying a high signal to **CEn** input. In the standby mode, the outputs are not in a high impedance state. Typically 25uA (100uA at Max.) of current is consumed in the standby mode. During power-up, about 400uA of peak current can flow when VCC rises to the stabilized level. This “peak current during power-up” can be completely suppressed down by letting the device stay at “deep power-down mode” during power-up. Keep PDOWn at Low during power-up. Refer to Fig. 14.

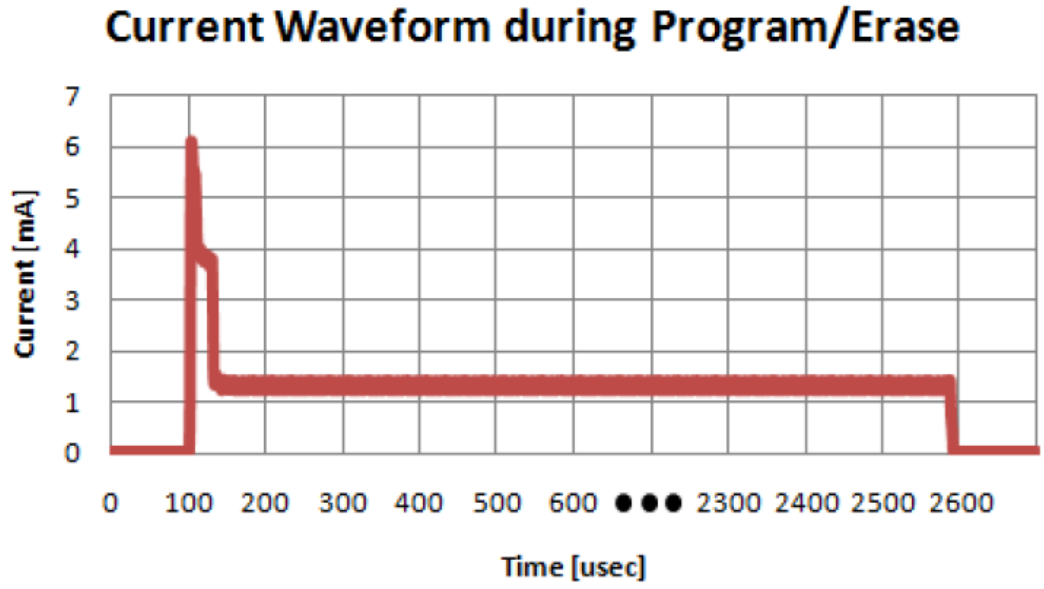
Fig. 14 Peak current during power-up



14. Peak current during write operation

At maximum, 6mA of peak current can flow at an initial stage of write operation. This is caused by initially activating charge pump circuit to generate high voltages for cell array into which data will be written. However, this peak-current is rapidly suppressed down to less than 1.5mA as soon as the internal charge pump operation is stabilized.
Even if the supplying current is limited to 4mA, actual write operation is not critically affected. This is because 4msec of write time is long enough. Refer to Fig. 15.

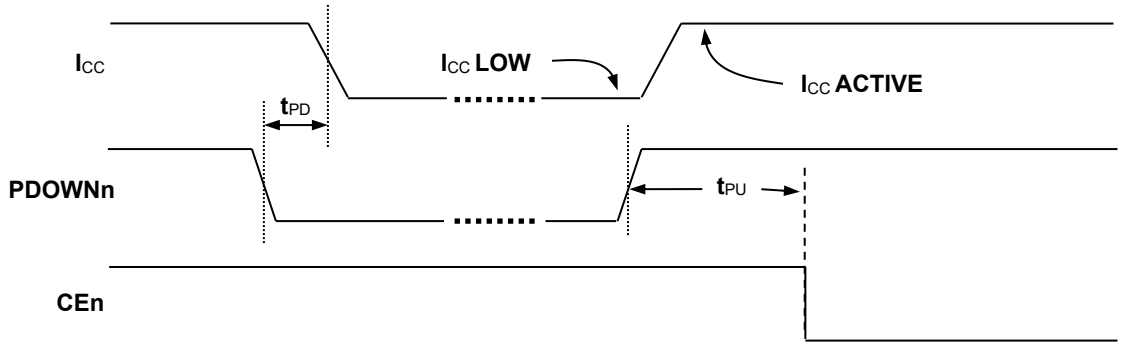
Fig. 15 Peak current during write operation



15. Deep power-down mode

In case that extremely small power consumption is required in stand-by mode, the deep power-down mode is recommended. In this mode, typically **less than 1uA** is consumed. By just asserting low to PDOWNn input, the device can be forced to enter the deep mode. In this mode, all circuits are completely turned off. At the same time, all internal registers and latches including the **page buffer** are reset to all “0”. Furthermore, any in-progress operation (such as write operation) is immediately terminated. However, **100usec of wake-up time** is required for the device to return to the normal read mode after the device gets out of this deep power-down mode.

Fig. 16 Deep power-down mode



16. Device Reset

The device can be reset by asserting RSTn **(at least 20nsec, tRSTL**), regardless of other control signals. All internal registers and latches including the **page buffers** are completely cleared (initialized) and all outputs turn to X (unknown) by the device reset. While the device stays at reset status (RSTn at low), all internal circuits of the device are disabled. So, in this reset status, just intrinsic leakage current (called “stand-by current”) is consumed over the entire device, like the stand-by mode.

In order to guarantee the safe device operation during power-up, the device needs to stay at reset status by keeping RSTn low until the power-supply is fully ramped up and finally stabilized. Refer to Fig.17. If the device is not kept properly at reset during power-up, some undesired result may take place by unstable input signals or noises generated during power-up.
After power-up, the device automatically enters the read mode. But, 100usec of wait-time (tSR) is required for the device to get ready for read even if the device gets out of “device reset” by releasing RSTn.

In case that RSTn is asserted during the write operation, the write operation will be immediately interrupted and terminated. Therefore, they (the interrupted operations) need to be reinitiated to ensure data integrity which may have been corrupted by immediate termination of the write process.

Fig. 17 Device reset during power-up and Power-down

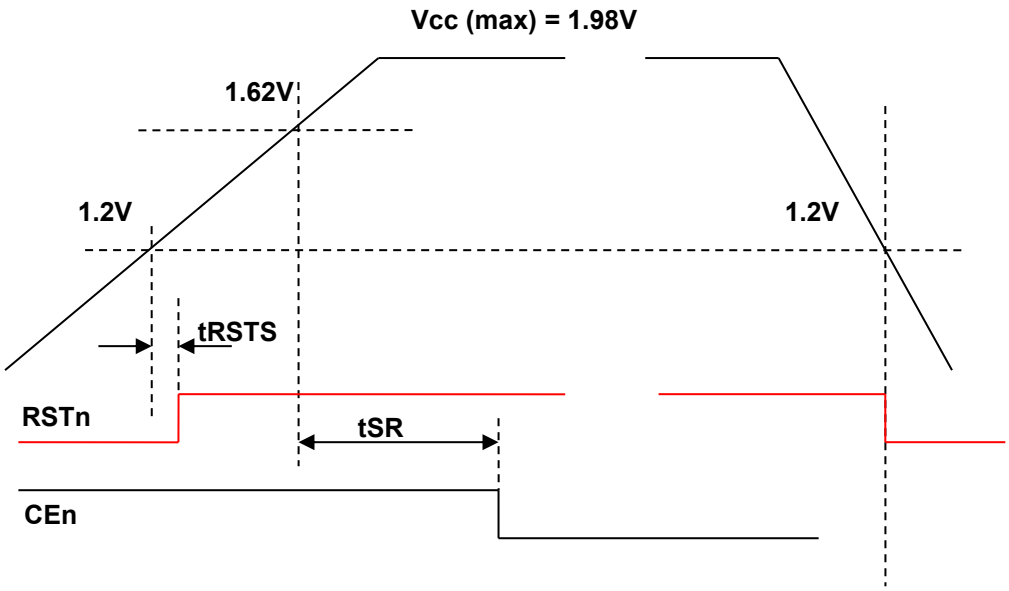


Table 14.

Symbol	Parameter	Min.	Typ.	Max.	Unit
tPD	Power Down Time			5	us
tPU	Power Up Time	100			us
tRSTS	RSTn Set Time	0			ns
tRSTL	RSTn Low Width Time	20			ns
tSR	System Ready during power up	100			us

17. DC Operating Characteristics

Table 16.

Description	Symbol	Condition		Min	Typ	Max	Unit
Operation Temperature	Temp.	Read		-40	25	85	℃
		Write		-20	25	85	℃
Power Supply Voltage	V_{DD}			1.62	1.8	1.98	V
Stand By Current	I_{SB}	CEn= High	G		30	100	μA
			W		30	60	μA
Power Down Current	I_{pd}	PDOWNn=Low	G		1	70	μA
			W		1	30	μA
Read Current (Output Load less than 0.3pF)	I_{CC}	1MHz			1	2	mA
		10MHz			2	4	mA
Write Current	I_{WR}	Erase or Program			1	2	mA
Input Low Voltage	V_{IL}			-0.3	0	0.1	V
Input High Voltage	V_{IH}			V_{DD} -0.3	V_{DD}	V_{DD} +0.3	V
Output High Voltage	V_{OH}	Ioh=1uA		$0.9XV_{DD}$		$1.1XV_{DD}$	V
Output Low Voltage	V_{OL}	Iol=1uA		-0.3		$0.1XV_{DD}$	V
Input Capacitance	C_{IN}	V_{IL}=0V; Temp. 25℃				0.1	pF
Output Capacitance	C_{OUT}	V_{IL}=0V; Temp. 25℃				0.3	pF

(Note) G (WC18EX2G), W (WC18EX2W)

Revisions

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Revised by S.D Kim (sdkim@Jeenix.com)

Note

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